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(54) Drive circuit for cholesteric liquid crystal displays

(57) Apparatus for driving a cholesteric liquid crystal display wherein the display includes cholesteric liquid crystals having a first planar reflective state and a second transparent focal conic state, which is respectively responsive to different applied fields; an addressing structure having rows and columns of conductors arranged so that when a column and a row overlap, they define a selectable pixel or segment to be viewable or non-viewable; the apparatus being adapted to switch between a first and a second fixed voltage.

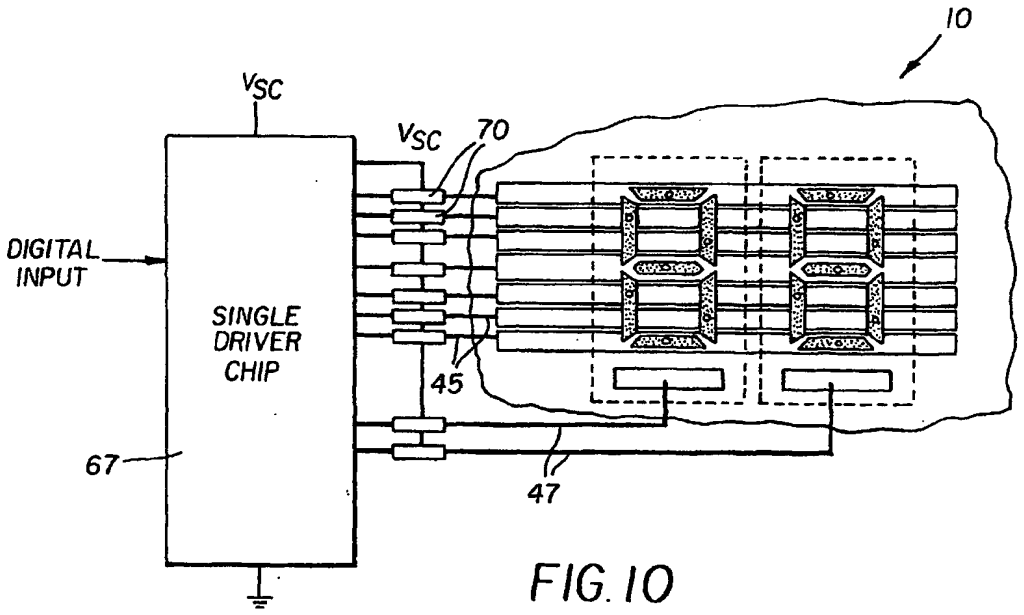

FIG. 10

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FIG. 1 is an isometric partial view of a cholesteric liquid crystal display made in accordance with the present invention;
FIG. 2 is an assembly diagram of the display in FIG. 1 being attached to a card;
FIG. 3A is a schematic sectional view of a chiral nematic material in a planar state reflecting light;
FIG. 3B is a schematic sectional view of a chiral nematic material in a focal conic state transmitting light;
FIG. 4 is a plot of the response of a first polymer dispersed cholesteric material to a pulsed electrical field with a first set of imposed voltages;
FIG. 5 is a schematic representation of a matrix array of cholesteric liquid crystal elements;
FIG. 6 is a front view of the display of FIG.1;
FIG. 7 is an electrical schematic of prior art drive for the display of FIG. 1;
FIG. 8 is a schematic of the prior art drive of FIG. 7;
FIG. 9 is a diagram of the waveforms generated by prior art to drive the display of FIG. 1;
FIG. 10 is an electrical schematic the new drive scheme operating on the display of FIG. 1;
FIG. 11 is a diagram of the waveforms generated by the current invention to drive the display of FIG. 1;
FIG. 12 is detail of a first embodiment of the drive in FIG.10; and
FIG. 13 is detail of a second embodiment of the drive in FIG.10.

[0013] FIG. 1 is an isometric partial view of a new structure for a display 10 made in accordance with the invention. Display 10 includes a flexible substrate 15, which is a thin transparent polymeric material, such as Kodak Estar film base formed of polyester plastic that has a thickness of between 20 and 200 microns. In an exemplary embodiment, substrate 15 can be a 125 micron thick sheet of polyester film base. Other polymers, such as transparent polycarbonate, can also be used.

[0014] First patterned conductors 20 are formed over substrate 15. First patterned conductors 20 can be tin-oxide or indium-tin-oxide (ITO), with ITO being the preferred material. Typically the material of first patterned conductors 20 is sputtered as a layer over substrate 15 having a resistance of less than 250 ohms per square. The layer is then patterned to form first patterned conductors 20 in any well known manner. Alternatively, first patterned conductors 20 can be an opaque electrical conductor material such as copper, aluminum or nickel. If first patterned conductors 20 are opaque metal, the metal can be a metal oxide to create light absorbing first patterned conductors 20. First patterned conductors 20 are formed in the conductive layer by conventional lithographic or laser etching means.

[0015] A polymer dispersed cholesteric layer 30 overlays first patterned conductors 20. Polymer dispersed cholesteric layer 30 includes a polymeric dispersed cholesteric liquid crystal material, such as those disclosed in US-A-5,695,682, the disclosure of which is incorporated by reference. Application of electrical fields of various intensity and duration can drive a chiral nematic material (cholesteric) into a reflective state, to a transmissive state, or an intermediate state. These materials have the advantage of maintaining a given state indefinitely after the field is removed. Cholesteric liquid crystal materials can be Merck BL112, BL118 or BL126, available from E.M. Industries of Hawthorne, N. Y.

[0016] In the preferred embodiment, polymer dispersed cholesteric layer 30 is E.M. Industries' cholesteric material BL-118 dispersed in deionized photographic gelatin. The liquid crystal material is dispersed at 8% concentration in a 5% deionized gelatin aqueous solution. The mixture is dispersed to create 10 micron diameter domains of the liquid crystal in aqueous suspension. The material is coated over a patterned ITO polyester sheet to provide a 9 micron thick polymer dispersed cholesteric coating. Other organic binders such as polyvinyl alcohol (PVA) or polyethylene oxide (PEO) can be used. Such compounds are machine coatable on equipment associated with photographic films.

[0017] Second patterned conductors 40 overlay polymer dispersed cholesteric layer 30. Second patterned conductors 40 should have sufficient conductivity to carry a field across polymer dispersed cholesteric layer 30. Second patterned conductors 40 can be formed in a vacuum environment using materials such as aluminum, tin, silver, platinum, carbon, tungsten, molybdenum, tin or indium or combinations thereof. The second patterned conductors 40 are as shown in the form of a deposited layer. Oxides of said metals can be used to darken second patterned conductors 40. The metal material can be excited by energy from resistance heating, cathodic arc, electron beam, sputtering, or magnetron excitation. Tin-oxide or indium-tin oxide coatings permit second patterned conductors 40 to be transparent.

[0018] In a preferred embodiment, second patterned conductors 40 are printed conductive ink such as Electrodag 423SS screen printable electrical conductive material from Acheson Corporation. Such printed materials are finely divided graphite particles in a thermoplastic resin. The second patterned conductors 40 are formed using printed inks to reduce cost display. The use of a flexible support for substrate 15, laser etching to form first patterned conductors 20, machine coating polymer dispersed cholesteric layer 30, and printing second patterned conductors 40 permits the fabrication of very low cost memory displays. Small displays formed using these methods can be used as electronically rewritable tags for inexpensive, limited rewrite applications.

[0019] A dielectric can be printed over second patterned conductors 40 and have openings through vias that permit interconnection between second patterned conductors 40 and conductive traces that form traces to define rows 45. Rows 45 can be the same screen printed

40 connected to row 45 overlap, they define a selectable pixel or segment to be viewable or non-viewable.

[0026] FIG. 7 is an electrical schematic of typical prior art used to drive the display of FIG. 1 based on the teaching in US-A-5,644,330. Four power supplies are needed to supply +Vc, -Vc, +VR, -VR and ground. Each line output of must switch one of three voltages to each line of a matrix display. Conventional bipolar drive schemes, as disclosed in US-A-5,748,277, require the use of expensive analog switching elements 55 as found in a Supertex HV204 8-Channel High Voltage Analog Switch. One analog switch is required for each voltage applied to each trace of the display. Such expensive chips prohibit low cost commercialization. Even more complex switching schemes have been proposed which increase the number of power supplies and analog switches are disclosed in other patents, such as US-A-5,748,277.

[0027] FIG. 8 is a more detailed view of the drive used in FIG. 7. Four power supplies are needed to supply +Vc, -Vc, +VR, -VR and ground. Separate drive chips, row driver 60 and a column driver 65 are required for the rows and column voltages. Digital data is fed to row driver 60 and column driver 65. A set of shift registers in the drivers receives and latches binary state data. The latched data control the operation of switches 55, which are high voltage bilateral DMOS switches. Multiple switches 55 must be combined to provide multiple voltages to each row or column of display 10.

[0028] FIG. 9 is a diagram of the waveforms used by prior art using the bipolar drive scheme shown in FIG. 7. A bipolar row voltage VR can be applied to a selected row, while a bipolar column voltage Vc is applied either in phase or out of phase with the row voltage VR. If the bipolar voltages are out of phase, the pixel will experience alternating bipolar high pixel voltage Vp corresponding to V4 and be written into the planar state (P). If the two voltages are in phase, then a pixel experiences lower alternating bipolar pixel voltage Vp corresponding to V3 and is written into the focal conic state (FC). Columns 47 held at a ground state (0) experience a bipolar alternating column voltage Vc as an alternating AC field equivalent to half the voltage difference between V4 and V3. Column voltage is less than disturbance voltage V1 to preserve the image state of unwritten, grounded rows.

[0029] A schematic of a drive scheme in accordance with the current invention is shown in FIG. 10. A single driver chip 67 is used to apply unipolar fields to display 10 using passive components 70. Instead of expensive analog switches, the new drive uses simple push-pull outputs to switch a set of outputs between a fixed high voltage, in the exemplary embodiment 90 volts, and second lower voltage, which in the example is ground. Such a chip can be the STV7699 plasma display driver from ST Microelectronics, which has a set of 64 output lines controlled by a set of shift registers 50 which switches each output 56 between single chip voltage or ground. In the exemplary embodiment, disturbance voltage V1 is 20 volts, focal conic voltage V3 is 60 volts and planar voltage V4 is 90 volts.

[0030] FIG. 11 is a diagram of the waveforms used to write display 10 using the new drive scheme. One output of single driver chip 67 is used to supply a switchable single chip voltage Vsc, in the exemplary embodiment 90 volts, to passive components 70. When display 10 is not being written, single chip voltage Vsc is supplied to passive components 70 kept at ground. When 90 volt is "ON" to supply passive components 70, row voltage VR is shifted to 15 volts. The 15 volts act as the ground state for the writing process. Column voltages Vc being at true ground nominally applies -15 volts potential for pixel voltage Vp. That voltage is below disturbance voltage V1. A row of data is written by switching row voltage VR high to 90 volts. Column voltage Vc is switched to 30 volts to convert cholesteric liquid crystal into the focal conic state (FC) or remains grounded to convert cholesteric liquid crystal into the planar state (P). Unwritten rows held at zero volts until they experience either -15 and +15 volts from column voltage Vc as rows are written. The 15 volt ripple is below disturbance voltage V1, and image data in unwritten rows are not disturbed. At the end of writing, all outputs of single driver chip 67 are set to the ground to the "OFF" state, and no fields are present on display 10.

[0031] A first configuration of passive components 70 is shown in FIG. 12. Passive components 70 include sets of resistors which act as a voltage divider to provide select output voltages from fixed single chip voltage Vsc. A first set of resistors on each row output causes row voltage VR to switch between 90 and 15 volts. One output of single driver chip 67 supplies single chip voltage Vsc to passive components 70 used to generate row voltage VR. Supplying single chip voltage Vsc through a dedicated output line permits display 10 to be grounded after writing by switching all outputs to ground. A second set of resistors on each column output switches column voltage Vc between 0 and 30 volts. Passive components 70 provide one of two voltages for a column and one of the two voltages for a row from a common fixed single chip voltage Vsc. The voltages supplied to a particular pixel or segment provide a unipolar field that causes such pixel or segment to be in a transparent or reflective state.

[0032] A second scheme using passive components 70 is shown in FIG. 13. The second configuration use a set of resistors and a diode 71 to provide the correct row voltages VR and column voltages Vc. A set of resistors provides the intermediate voltage on each output, and diodes 71 eliminate switching to ground potential for row voltages VR and switching to single chip voltage Vsc for column voltages. The diode configuration permits the drive to be used with displays 10 having high capacitance. With higher display capacitance, the rise and fall time of the applied voltages increases affects display image quality. Replacing each series resistor from the first embodiment with diodes 71 permits fast rise and fall

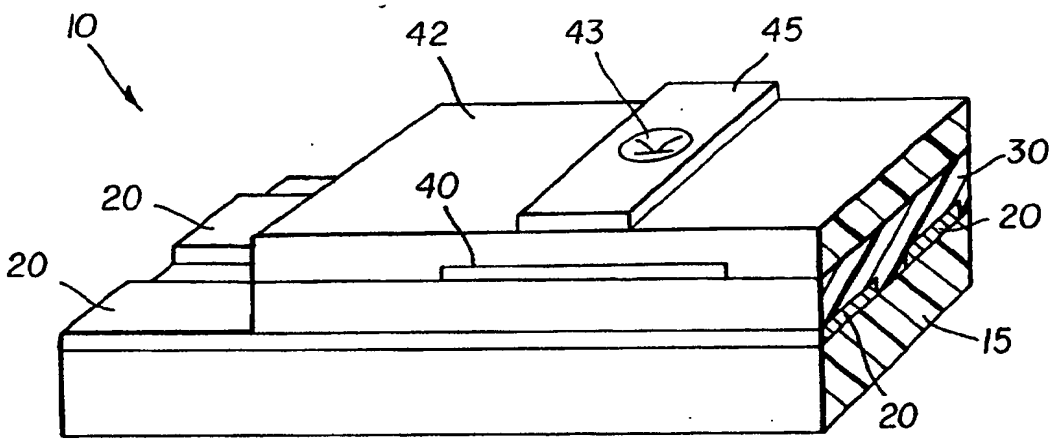

FIG. 1

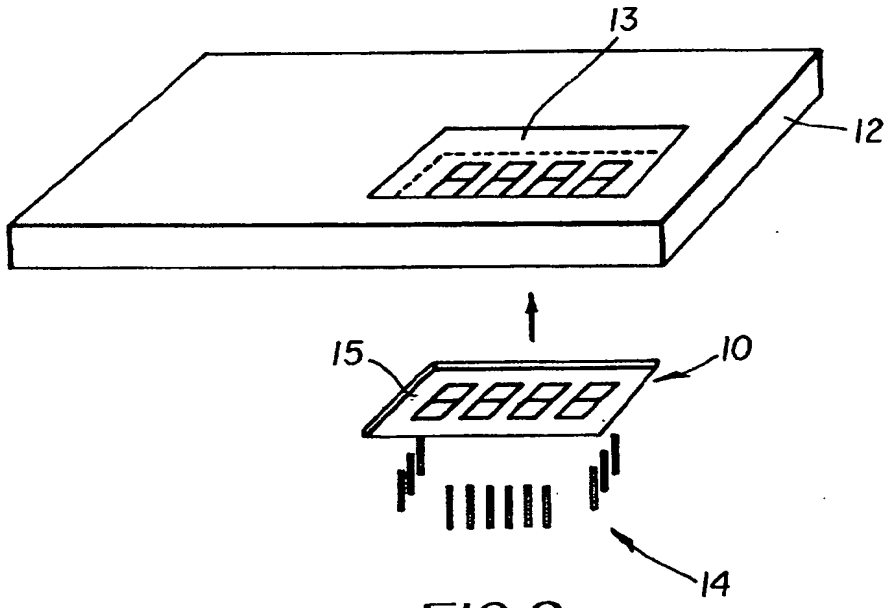

FIG. 2

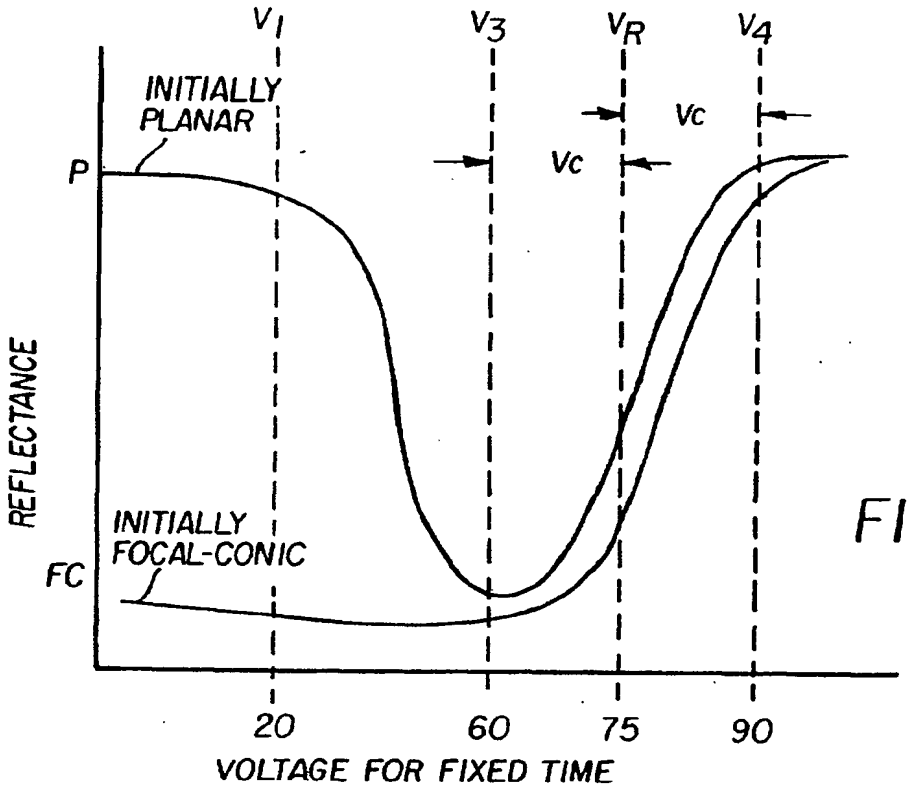
V1
V3
VR
V4
INITIALLY PLANAR
P
Vc
Vc
REFLECTANCE
INITIALLY FOCAL-CONIC
FC
20
60
75
90
VOLTAGE FOR FIXED TIME

FIG. 4

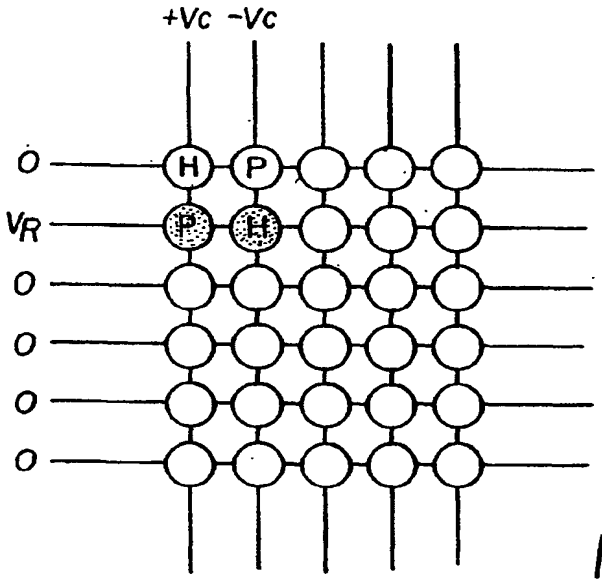
+Vc
-Vc
0
VR
0
0
0
0
H
P
P
H

FIG. 5

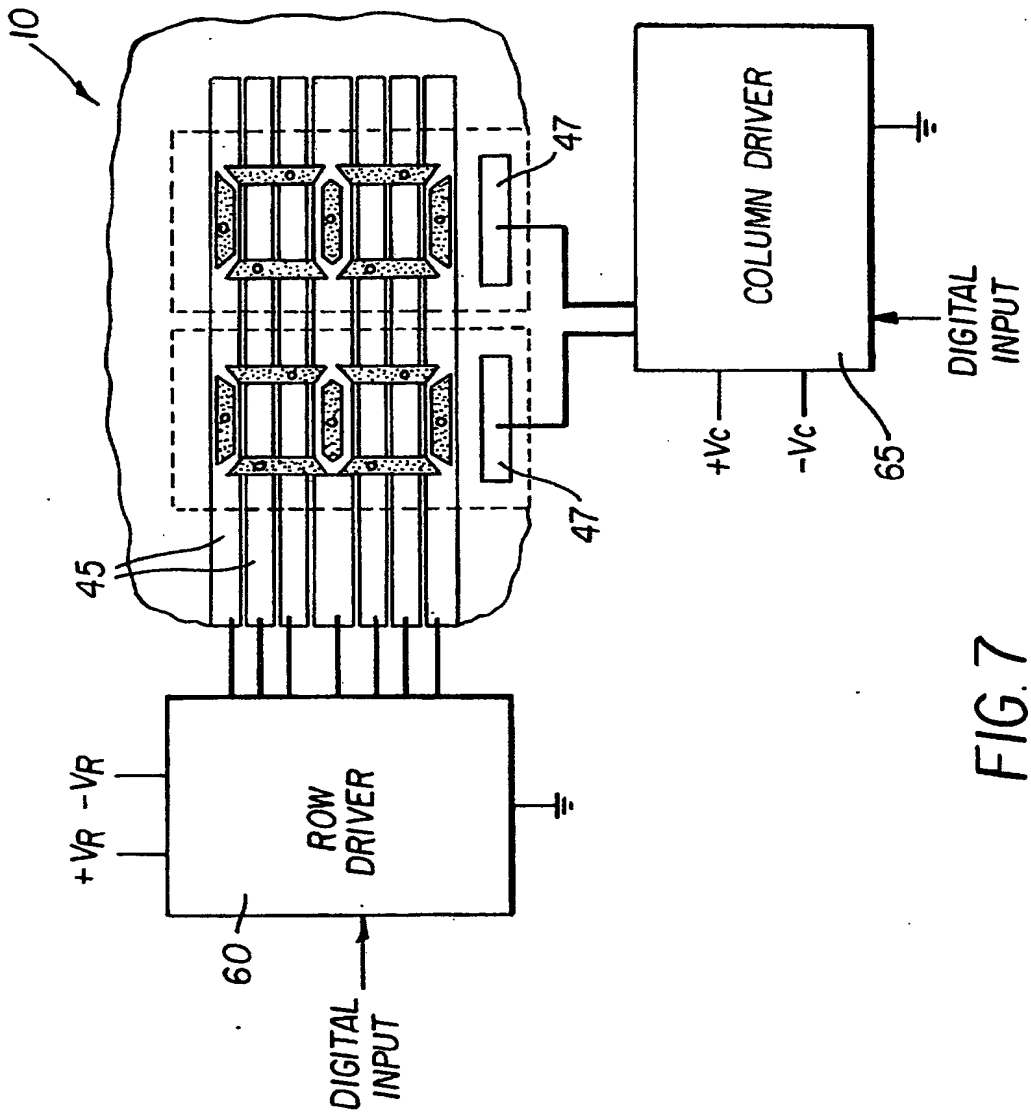
10
47
47
45
COLUMN DRIVER
DIGITAL INPUT
+Vc
-Vc
65
+VR -VR
ROW DRIVER
60
DIGITAL INPUT

FIG. 7

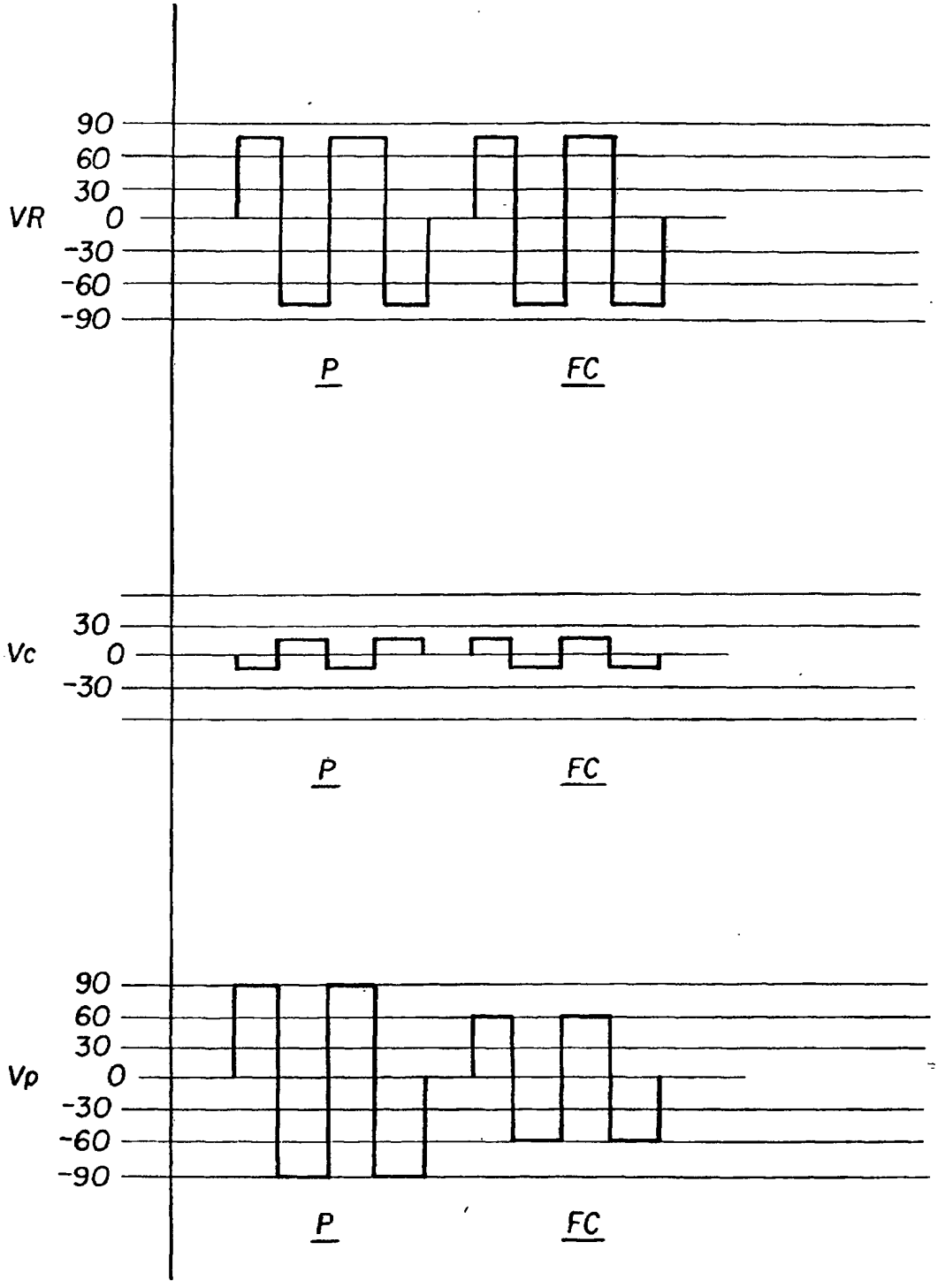

FIG. 9

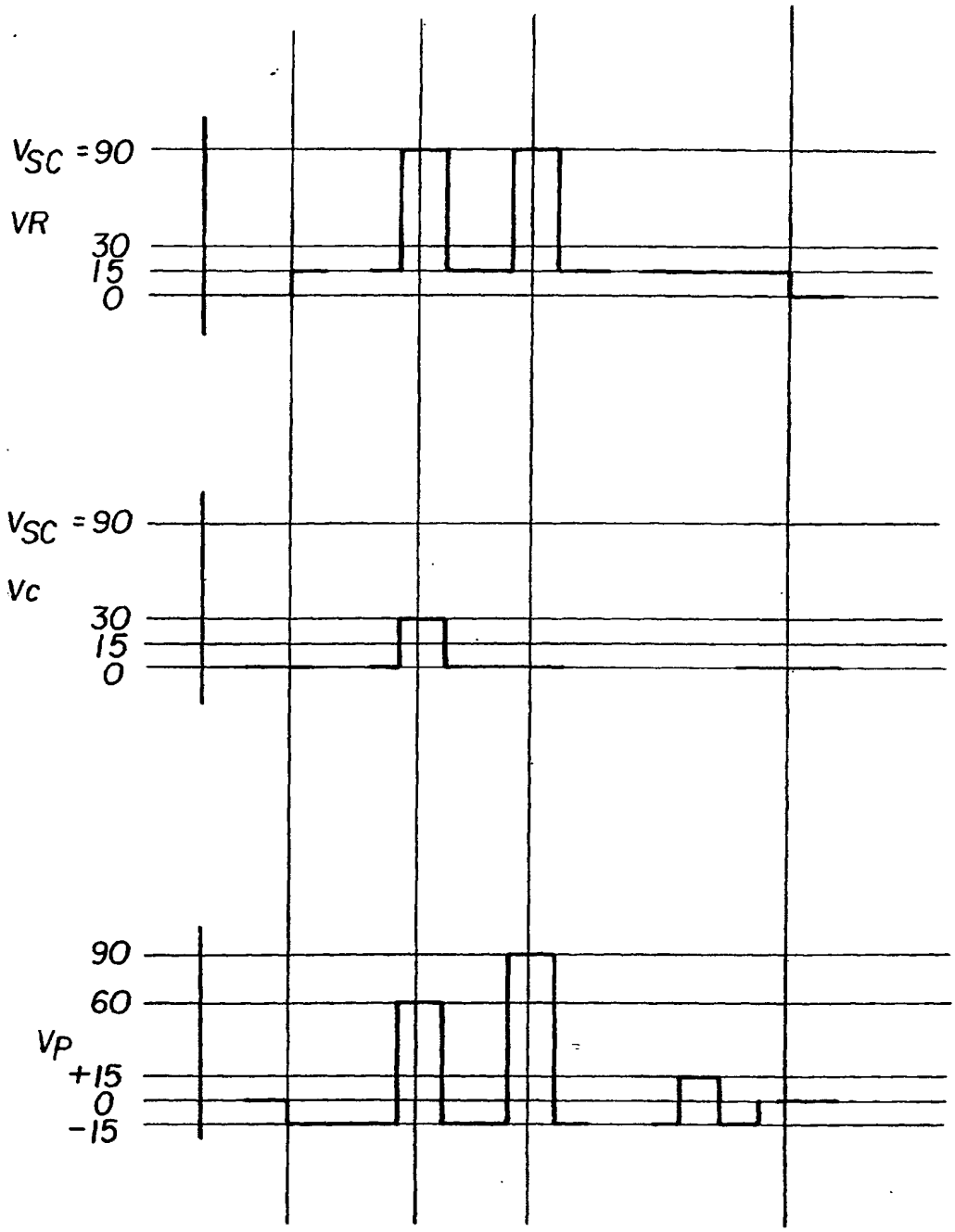

FIG. 11

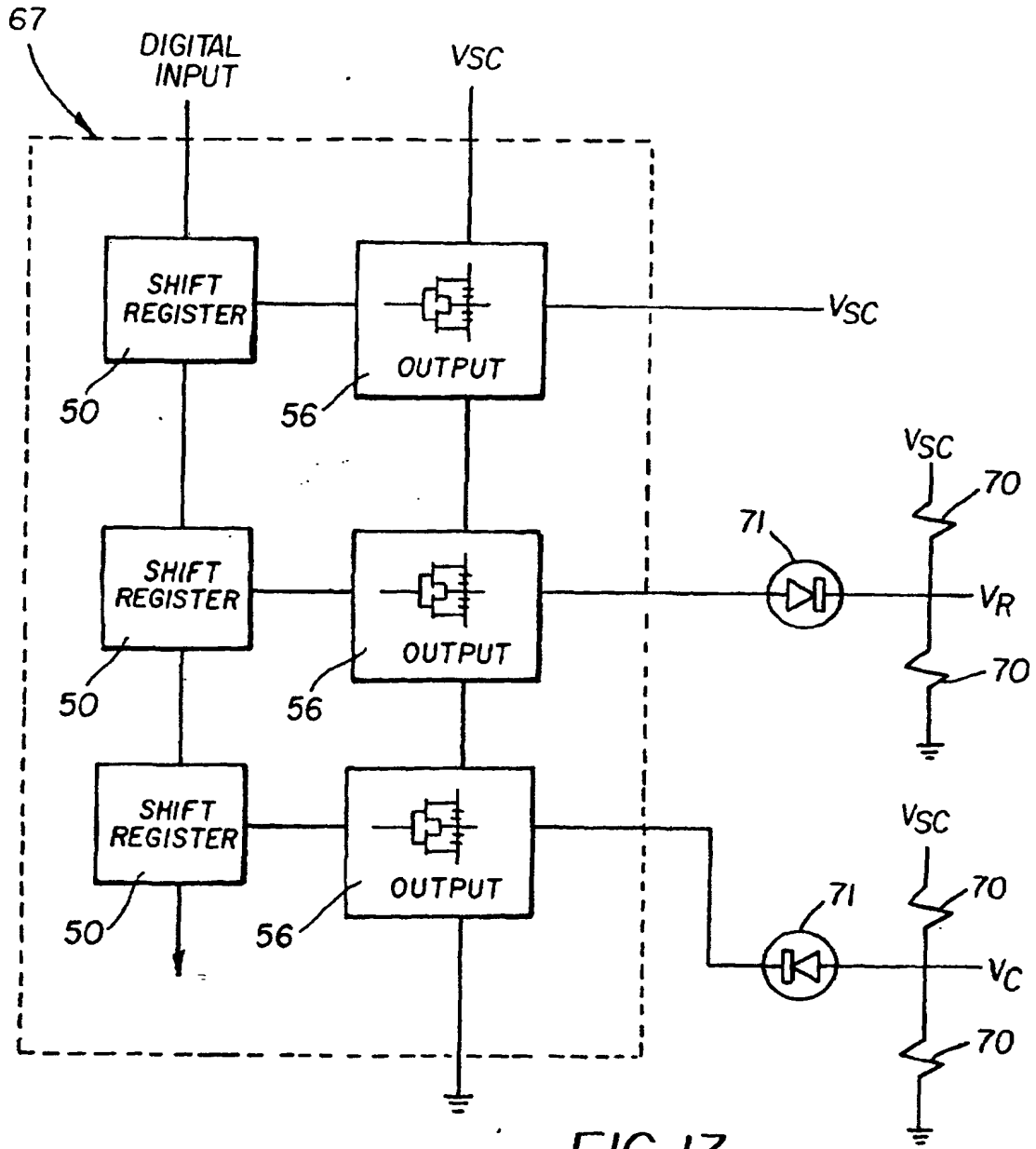
67
DIGITAL INPUT
VSC
SHIFT REGISTER
OUTPUT
VSC
50
56
SHIFT REGISTER
OUTPUT
50
56
SHIFT REGISTER
OUTPUT
50
56
VSC
70
71
VR
70
VSC
70
71
VC
70

FIG. 13

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 02 07 6708

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
Y,D	7699-01.EPS, Product Preview, STV7699, Plasma Display Data Driver, ST Microelectronics, January 1999 XP002201715 * the whole document *	2	

TECHNICAL FIELDS SEARCHED (Int.Cl.7)

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
MUNICH	12 June 2002	Harke, M

CATEGORY OF CITED DOCUMENTS

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